Hittite Microwave

Use of HMCAD1520 Precision Mode from 105 to 122.8 MSPS

Operating HMCAD1520 in precision mode in the 105 to 122.8MSPS range

- ✓ *The HMCAD1520 can be operated above the 105MSPS defined in the datasheet, given the following constrains*
  - ✓ *LVDS must be set to Dual 8 bit (Gives 2*8=16bit for each channel output. Data in the 14 MSB bits)*
  - ✓ *Analog supply voltage should be set to 1.9V±0.1V*
  - ✓ *For FS>115MSPS: Adc_current should be set to 90%. This is to avoid current saturation at the highest sample rate.*
- ✓ *This presentation will show the performance of HMCAD1520PM given these constraints*

Measurement setup

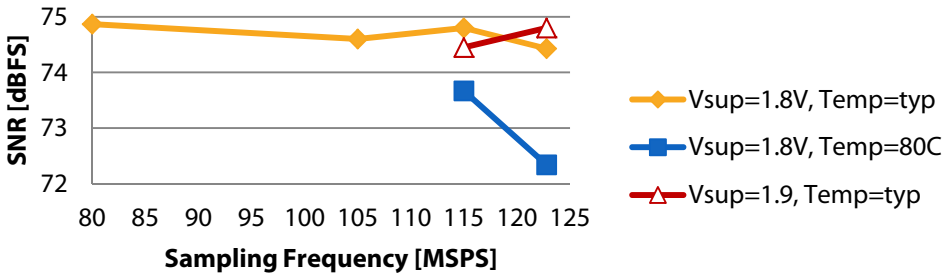
- ✓ *Supply voltage: 1.8V and 1.9V*
- ✓ *Temperature: 25ºC and 80ºC*
- ✓ *LVDS: Dual 8-bit1.5mA RSDS Mode*
- ✓ *ADC_curr register settings*
  - ✓ *80-115MSPS: Nominal*
  - ✓ *122.8MSPS: Nominal-10% (90%)*
- ✓ *Input signal: -1dBFS 70MHz sinewave*

Measurement conclusions

- ✓ In the 80-115MSPS range the performance is:
  - ✓ Typical conditions:
    - ✓ SNR>74dBFS, SNDR>73dBFS, SFDR>80dBc
  - ✓ High temperature
    - ✓ SNR>73dBFS, SNDR>72dBFS, SFDR>80dBc
- ✓ In the 115-122.8MSPS range the performance is:
  - ✓ Typical conditions:
    - ✓ SNR>74dBFS, SNDR>73dBFS, SFDR>80dBc
  - ✓ High temperature
    - ✓ SNR>72dBFS, SNDR>70dBFS, SFDR>79dBc

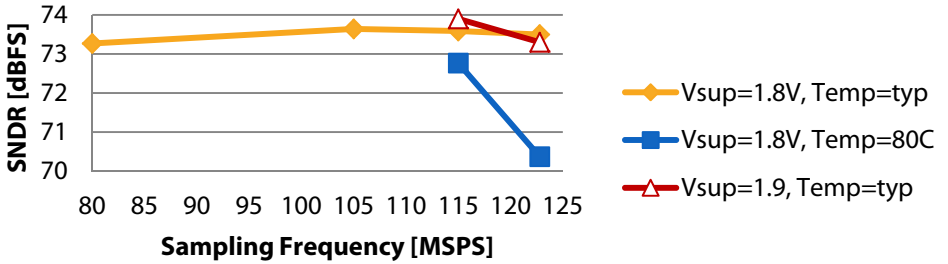
SNR vs Sample rate

Fin=70MHz, Ain=-1dBFS



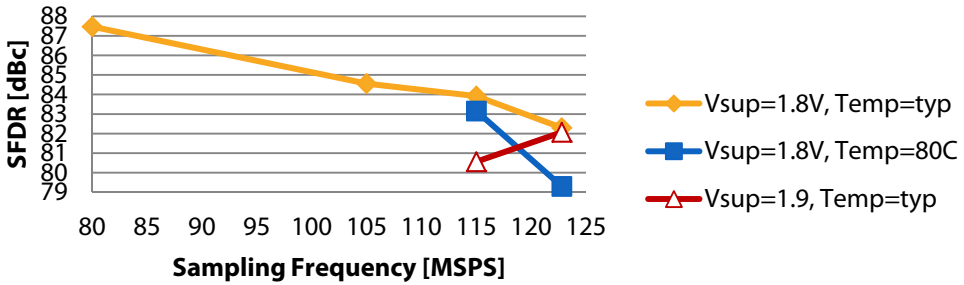
SNDR vs Sample rate

Fin=70MHz, Ain=-1dBFS



SFDR vs Sample rate

Fin=70MHz, Ain=-1dBFS



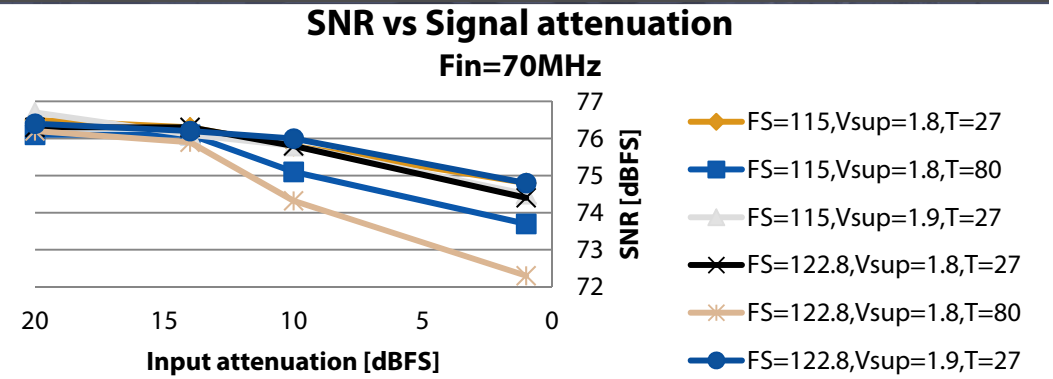
HMCAD1520-Precision Mode 105 to 122.8 MSPS
SNR, SNDR and SFDR at -20 to -1dBFS input signal level

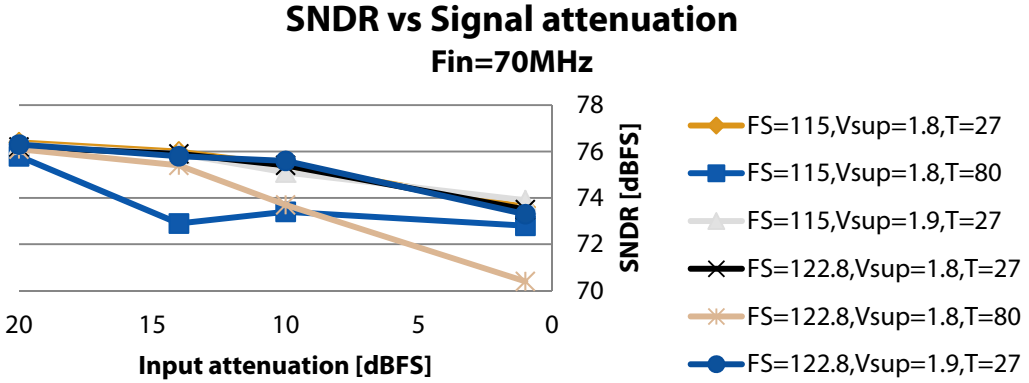
Measurement setup

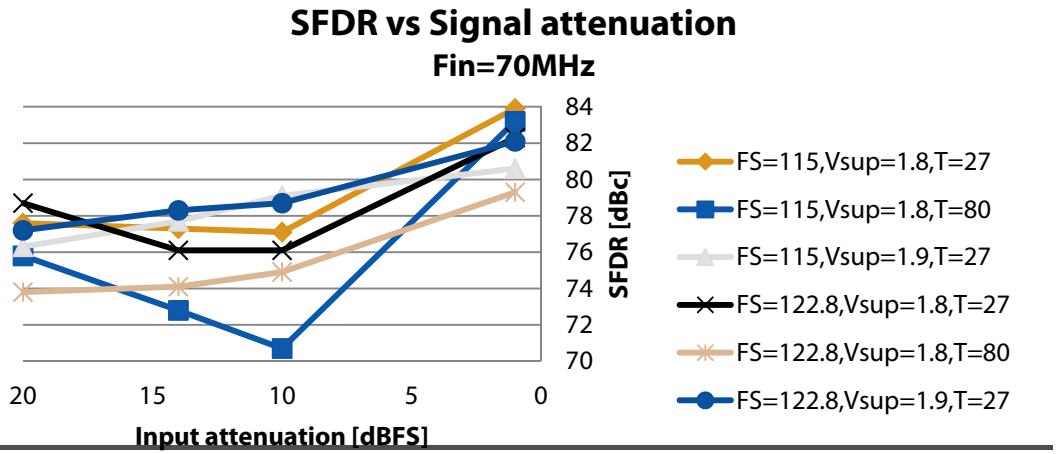
- ✓ *Supply voltage: 1.8V and 1.9V*
- ✓ *Temperature: 25ºC and 80ºC*
- ✓ *LVDS: Dual 8-bit1.5mA RSDS Mode*
- ✓ *ADC_curr register settings*
  - ✓ *115MSPS: Nominal*
  - ✓ *122.8MSPS: Nominal-10% (90%)*
- ✓ *Input signal: -1dBFS 70MHz sinewave*

Measurement conclusions

- ✓ SNR and SNDR dominated by -1dBFS with results as gicen in previons slide
- ✓ When input signal decrease, SNR and SNDR will slightly improve
- ✓ SFDR is >75dBc in the entire -20 to -1dBFS range given typical temperature
- ✓ At high temperature and -20 to -10 dFBS input signal, the SFDR is between 70-75dBc



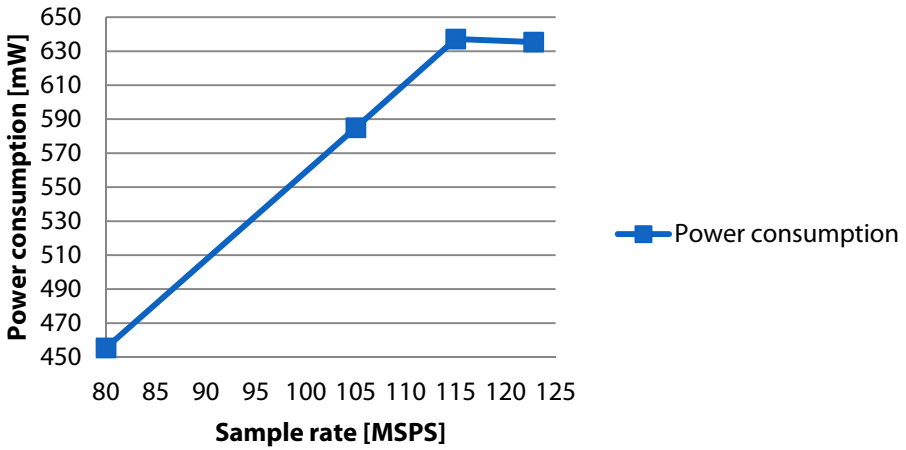




Measurement setup

- ✓ *Supply voltage: 1.8V*
- ✓ *Temperature: 25°C*
- ✓ *LVDS: 1.5mA RSDS Mode*
- ✓ *ADC_curr register settings*
  - ✓ *80-115MSPS: Nominal*
  - ✓ *122.8MSPS: Nominal-10% (90%)*
- ✓ *Input signal: -1dBFS 70MHz sinewave on ch 1*

Power consumption vs Sample rate



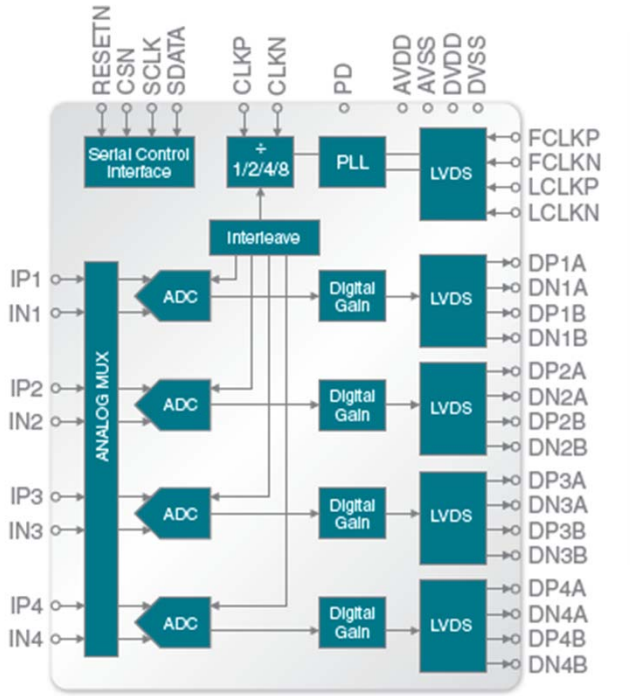
Measurement conclusions

- ✓ ADC power consumption scales linearly from 455 to 635mW over the 80 to 115MSPS range
- ✓ At 122.8MSPS , the increase in current due to increased sample rate, is compensated by reducing the ADC current SPI setting. This eliminates current saturation in the analog circuitry

Part Number	Function / Mode	Resolution (bits)	Sample Rate (MSPS)	Power Dissipation[2][3]	SNR (dBFS)	SFDR (dBc)	Package
HMCAD1520	High Speed Single Channel	12	640	490 mW	70	60 / 75 [1]	LP7DE
	High Speed Dual Channel	12	320	490 mW	70	60 / 78 [1]	
	High Speed Quad Channel	12	160	490 mW	70	60 / 78 [1]	
	Precision Quad Channel	14	105	603 mW	74	83	
	Precision Quad Channel	14	80	530 mW	75	85	

Features

- ✓ *Multiple Modes*
  - ✓ *Single channel 12-bit up to 640 MSPS*
  - ✓ *Dual channel 12-bit up to 320 MSPS*
  - ✓ *Quad channel 12-bit up to 160 MSPS*
  - ✓ *Quad channel 14-bit up to 105 MSPS*
- ✓ *SPI Configurable Operational Modes*
- ✓ *SPI Configurable Number of Channels*
- ✓ *1µs Switching Time Between Configurations*
- ✓ *Internal 1X to 8X Clock Divider*
- ✓ *LVDS output*
  - ✓ *Full robustness in RSDS (Low Current) Mode*
- ✓ *Ultra Low Power Dissipation*
  - ✓ *Dynamic power vs. sample rate scaling*
- ✓ *Coarse & Fine Gain Control*
- ✓ *48 Pin QFN Package*



[1] Excluding Interleaving Spurs
[2] Supply Voltage (Vdd) +1.8 Vdc Analog Supply (Avdd) and +1.8Vdc Digital Supply (Dvdd)
[3] Output Supply Voltage (OVdd) +1.7 to +3.6 Vdc

Operating HMCAD1520 in precision mode in the 105 to 122.8MSPS range

- ✓ *It The HMCAD1520 can be operated above the 105MSPS defined in the datasheet, given the following constrains*
  - ✓ *LVDS must be set to Dual 8 bit (Gives 2*8=16bit for each channel output. Data in the 14 MSB bits)*
  - ✓ *Analog supply voltage should be set to 1.9V±0.1V*
  - ✓ *For FS>115MSPS: Adc_current should be set to 90%. This is to avoid current saturation at the highest sample rate.*
- ✓ *Given these constraints, the performance of HMCAD1520 is comparable to the peroformance up to 105MSPS*